ABSTRACT OF THE DISCLOSURE

1   A video processor comprises a bit rate converter for converting an M-

2   bit input video signal to an N-bit output video signal by retaining gray levels

3   of the M-bit input video signal (where, N is smaller than M). A number of N-

4   bit input gray levels are mapped in a gamma correction memory to a number

5   of output gray levels. The output gray levels are distributed on a non-linear

6   curve complementary to a non-linear curve on which gray levels of a display

7   device are distributed. The memory delivers one of the output gray levels

8   when the N-bit output video signal of the bit rate converter corresponds to

9   one of the N-bit input gray levels. In one embodiment, the bit rate converter

10   truncates lower significant bits of the M-bit video signal, represents the

11   truncated bits by a different number of binary-1's, and distributes the binary-

12   1's over a varying number of subsequent frames depending on the value of

13   the truncated bits.